Code: 2298-60208
Ref. No.:3720-0001

JAPANESE PATENT OFFICE
PATENT JOURNAL
KOKAI PATENT APPLICATION NO. HEI 5[1993]-167004

Technical Disclosure Section

Int. Cl.[5]: H 01 L 25/065
25/07
25/18
H 01 L 25/08
21/92
H 01 L 21/321

Sequence Nos. for Office Use: 7220-4M
9168-4M

Application No.: Hei 3[1991]-327936

Application Date: December 12, 1991

Publication Date: July 2, 1993

No. of Claims: 3 (Total of 4 pages)

Examination Request: Not requested

SEMICONDUCTOR DEVICE

Inventor: Nobuharu Watanabe
Fujitsu, Ltd. 1015
Kamiodanaka, Nakahara-ku,
Kawasaki-shi,
Kanagawa-ken

Applicant: 000005223
Fujitsu, Ltd. 1015
Kamiodanaka, Nakahara-ku,
Kawasaki-shi,
Kanagawa-ken

Agent: Sadakazu Iketa

[There are no amendments to this patent.]

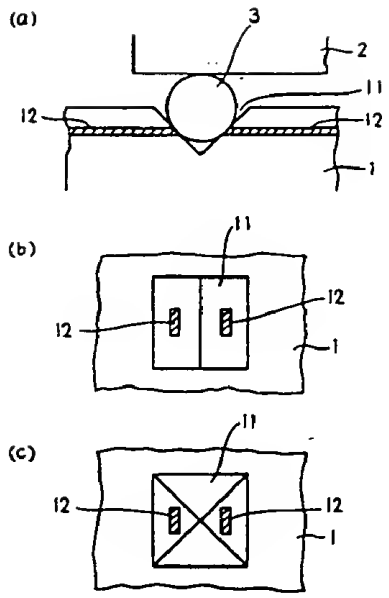
Abstract

Objective

To make the gap between the superimposed semiconductor chips small with regard to a semiconductor device composed as chip-on-chip.

Constitution

It is composed to have second semiconductor chip (2) connected to semiconductor chip (1) according to a bump on first semiconductor chip (1), and bump (3) with respect to said first or second semiconductor chip; here, first semiconductor chip (1) is connected to the end surface of wiring (12) exposed on the slanted surface of cavity (11) by one portion of bump (3) entering into cavity (11) provided to the semiconductor chip (1) via wiring (11) connected to bump (3) in the wiring layer of semiconductor chip (1). Cavity (11) is composed into a V groove or square conical groove. Bump (3) can be connected to the end surface of wiring (12) via conductor film (omitted from the figure) formed on the slanted surface of cavity (11).



Partial cross-sectional view and partial plane view of Application Example 1

Claims

1. A semiconductor device characterized by the fact that it has a second semiconductor chip connected to the first semiconductor chip according to a bump on the first semiconductor chip, and

said bump with respect to said first or second semiconductor chip is connected to the end surface of the wiring exposed on the slanted surface of a cavity by one portion of said bump entering into the cavity provided to the semiconductor chip via the wiring connected to the bump in the wiring layer of the semiconductor chip.

2. A semiconductor device noted in Claim 1, characterized by the fact that said bump is connected to the end surface of said wiring via a conductor film formed on the slanted surface of said cavity.

3. A semiconductor device noted in Claims 1 or 2, characterized by the fact that said cavity is a V groove or a square conical groove.

* * *